CLAIMS

1. (Currently amended) A semiconductor memory device, comprising:

a core block including a plurality of sub-arrays and a plurality of sense amplifier regions;

a plurality of first voltage supply lines capable of supplying a first operating voltage to the plurality of sense amplifier regions;

a plurality of second voltage supply lines capable of supplying a second operating voltage to the sense amplifier regions; and

a first charge storing region arranged at one side of the core block and including first charge storing means connected to the first and second voltage supply lines; and

a second charge storing region distinct from the first storing region arranged at an opposite side of the one side and including second charge storing means connected to the first and second voltage supply lines.

2. (Original) The memory device of claim 1 where a sense amplifier is formed at each of the sense amplifier regions, the sense amplifiers being supplied with the first and second operating voltages.

3. (Currently amended) The memory device of claim 1 where the first and second charge storing means comprises [[a]]first and second decoupling capacitors capable of preventing a power noise.

4. (Currently amended) The memory device of claim 3 where the first and second decoupling capacitors each comprises:

an active region formed at one side of the core block;

a plurality of first conductive films formed over the active region and connected to corresponding first voltage supply lines; and

a second conductive film formed over the active region and connected to the second voltage supply lines;

where the second conductive film is electrically connected to the active region through a plurality of contacts.

5. (Original) The memory device of claim 4
where the plurality of first conductive films is a polysilicon forming a gate; and
where the second conductive film is a polysilicon forming a bit line.

6. (Currently amended) A semiconductor memory device comprising:
a core block including a plurality of sub-arrays arranged in rows and columns and a plurality of sense amplifier regions each arranged between sub-arrays;
a plurality of first voltage supply lines capable of supplying a first operating voltage to the sense amplifier regions;
a plurality of second voltage supply lines capable of supplying a second operating voltage to the sense amplifier regions; and
a first charge storing region disposed at one side of the core block, the first charge storing region capable of connecting to the first supply lines;
a second charge storing region disposed at another side of the core block different than the one side, the second charge storing region capable of connecting to the second supply lines.

7. (Original) The memory device of claim 6
where a plurality of sense amplifiers are formed at each of the sense amplifier regions, the sense amplifiers being supplied with the first and second operating voltages.

8. (Original) The memory device of claim 6
where the first charge storing region comprises a first decoupling capacitor; and
where the second charge storing region comprises a second decoupling capacitor.

9. (Original) The memory device of claim 8 where the first decoupling capacitor comprises:
a first active region formed at the one side of the core block;
a plurality of first conductive films formed over the first active region and capable of connecting to the first voltage supply lines; and
a second conductive film formed over the first active region and capable of connecting to the second voltage supply lines;
where the second conductive film is capable of electrically connecting to the first active region through a plurality of contacts.

10. (Original) The memory device of claim 9 where the second decoupling capacitor comprises:

a second active region formed at the another side of the core block;

a plurality of third conductive films formed over the second active region and capable of connecting to corresponding first voltage supply lines; and

a fourth conductive film formed over the second active region and capable of connecting to the second voltage supply lines;

where the fourth conductive film is capable of electrically connecting to the second active region through a plurality of contacts.

11. (Original) The memory device of claim 10 comprising a row selector circuit disposed adjacent to a side of the core block.

12. (Original) The memory device of claim 10 comprising a column selector circuit disposed adjacent to a side of the core block.

13. (Original) The memory device of claim 10

where the first conductive films are a polysilicon material that form a gate; and

where the second conductive film is a polysilicon material that forms a bit line.

14. (Currently amended) A semiconductor memory device, comprising:

a core block including a plurality of sub-arrays arranged in rows and columns, a plurality of word line driving regions disposed between sub-arrays adjacent in a row direction, a plurality of sense amplifier regions each arranged between sub-arrays adjacent in a column direction, and a plurality of conjunction regions disposed between sense amplifier regions adjacent in the row direction;

a plurality of first voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a first operating voltage to the sense amplifier regions;

a plurality of second voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a second operating voltage to the sense amplifier regions; and

first and second charge storing regions respectively disposed at opposing sides of the core block;

where the first and second charge storing regions comprise first and second charge storing regions capable of connecting to first and second voltage supply lines, respectively.

15. (Original) The memory device of claim 14

where the sense amplifier regions include a plurality of sense amplifiers, the sense amplifiers being capable of receiving the first and second operating voltages.

16. (Currently amended) The memory device of claim [[8]]15 where the first charge storing means comprises:

a first decoupling capacitor including a first active region formed at one side of the core block;

a plurality of first conductive films formed over the first active region and capable of connecting to the first voltage supply lines, respectively; and

a second conductive film formed over the first active region and capable of connecting to the second voltage supply lines;

where the second conductive film is capable of electrically connecting to the first active region through a first plurality of contacts.

17. (Original) The memory device of claim 16 where the second charge storing means comprises:

a second decoupling capacitor including a second active region formed at another side of the core block;

a plurality of third conductive films formed over the second active region and capable of connecting to the first voltage supply lines; and

a fourth conductive film formed over the second active region and capable of connecting to the second voltage supply lines;

where the fourth conductive film is capable of electrically connecting to the second active region through a second plurality of contacts.

18. (Original) The memory device according to claim 17 comprising a row selector circuit disposed adjacent to the one side of the core block.

19. (Original) The memory device of claim 14 comprising:

a plurality of third voltage supply lines disposed on sense amplifier and word line driving regions, capable of supplying the first operating voltage to the sense amplifiers;

a plurality of fourth voltage supply lines disposed on sense amplifier and word line driving regions, capable of supplying the second operating voltage to the sense amplifiers.

20. (Original) The memory device of claim 19

where the first and third voltage supply lines are intersected and interconnected at the conjunction regions; and

where the second and fourth voltage supply lines are intersected and interconnected at the conjunction regions.

21. (Original) The memory device of claim 20 comprising third and fourth charge storing means connected to the third and fourth voltage supply lines, respectively.

22. (Currently amended) The memory device of claim 21 where the third and fourth charge storing means are disposed at other opposing sides of the core block different than the opposing sides.

23. (Currently amended) ~~The~~ A memory device ~~of claim 22,~~ comprising:

a core block including a plurality of sub-arrays arranged in rows and columns, a plurality of word line driving regions disposed between sub-arrays adjacent in a row direction, a plurality of sense amplifier regions each arranged between sub-arrays adjacent in a column direction, and a plurality of conjunction regions disposed between sense amplifier regions adjacent in the row direction;

a plurality of first voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a first operating voltage to the sense amplifier regions;

a plurality of second voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a second operating voltage to the sense amplifier regions;

first and second charge storing regions disposed at sides of the core block;

a column selector block disposed adjacent to the other sides of the core block;

a plurality of third voltage supply lines disposed on sense amplifier and word line driving regions, capable of supplying the first operating voltage to sense amplifiers;

a plurality of fourth voltage supply lines disposed on sense amplifier and word line driving regions, capable of supplying the second operating voltage to the sense amplifiers; and

third and fourth charge storing means connected to the third and fourth voltage supply lines, respectively;

where the first and third voltage supply lines are intersected and interconnected at the conjunction regions;

where the second and fourth voltage supply lines are intersected and interconnected at the conjunction regions;

where the first and second charge storing regions comprise first and second charge storing regions capable of connecting to first and second voltage supply lines, respectively; and

where the third and fourth charge storing means are disposed at other sides of the core block.

24. (Currently amended) ~~The~~ A memory device ~~of claim 22,~~ comprising:

a core block including a plurality of sub-arrays arranged in rows and columns, a plurality of word line driving regions disposed between sub-arrays adjacent in a row direction, a plurality of sense amplifier regions each arranged between sub-arrays adjacent in a column direction, and a plurality of conjunction regions disposed between sense amplifier regions adjacent in the row direction;

a plurality of first voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a first operating voltage to the sense amplifier regions;

a plurality of second voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a second operating voltage to the sense amplifier regions;

first and second charge storing regions disposed at sides of the core block;

a plurality of third voltage supply lines disposed on sense amplifier and word line driving regions, capable of supplying the first operating voltage to sense amplifiers;

a plurality of fourth voltage supply lines disposed on sense amplifier and word line driving regions, capable of supplying the second operating voltage to the sense amplifiers; and

third and fourth charge storing means connected to third and fourth voltage supply lines, respectively;

where the first and third voltage supply lines are intersected and interconnected at the conjunction regions;

where the second and fourth voltage supply lines are intersected and interconnected at the conjunction regions;

where the first and second charge storing regions comprise first and second charge storing regions capable of connecting to first and second voltage supply lines, respectively;

where the third and fourth charge storing means are disposed at other sides of the core block; and

where the third charge storing means comprises:

a third decoupling capacitor including a third active region formed at a third side of the core block;

a plurality of fifth conductive films formed over the third active region and capable of connecting to the third voltage supply lines; and

a sixth conductive film formed over the third active region and connected to the fourth voltage supply lines;

where the sixth conductive film is capable of electrically connecting to the third active region through a third plurality of contacts.

25. (Currently amended) The memory device of claim 24 where the second charge storing means comprises:

a fourth decoupling capacitor including a fourth active region formed at a fourth side of the core block;

a plurality of seventh conductive films formed over the fourth active region and capable of electrically connecting to the first voltage supply lines; and

an eighth conductive film formed over the fourth active region and capable of electrically connecting to the second voltage supply line;

where the ~~eigth~~ eighth conductive film is capable of electrically connecting to the fourth active region through a fourth plurality of contacts.

26. (Currently amended) ~~The~~ A semiconductor memory device ~~of claim 14~~, comprising:

a core block including a plurality of sub-arrays arranged in rows and columns, a plurality of word line driving regions disposed between sub-arrays adjacent in a row direction, a plurality of sense amplifier regions each arranged between sub-arrays adjacent in

a column direction, and a plurality of conjunction regions disposed between sense amplifier regions adjacent in the row direction;

a plurality of first voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a first operating voltage to the sense amplifier regions;

a plurality of second voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a second operating voltage to the sense amplifier regions; and

first and second charge storing regions disposed at sides of the core block;

where the first and second charge storing regions comprise first and second charge storing regions capable of connecting to first and second voltage supply lines, respectively;

where the first operating voltage is a supply voltage and the second operating voltage is a ground voltage.

27. (Original) A semiconductor memory device, comprising:

a core block including a plurality of sub-arrays, a plurality of word line driving regions disposed between sub-arrays, a plurality of sense amplifier regions each arranged between sub-arrays, each sense amplifier regions having a plurality of sense amplifiers, and a plurality of conjunction regions each disposed between sense amplifier regions;

a plurality of first voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a first operating voltage to the sense amplifier regions;

a plurality of second voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying a second operating voltage to the sense amplifier regions;

a plurality of third voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying the first operating voltage to sense amplifier regions;

a plurality of fourth voltage supply lines disposed on sense amplifier and conjunction regions, capable of supplying the second operating voltage to the sense amplifier regions; and

a charge storing region arranged to surround the core region and comprising charge storing means connected to the first, second, third, and fourth voltage supply lines.

28. (Original) The memory device of claim 27

where the first and third voltage supply lines are intersected and interconnected at the conjunction regions; and

where the second and fourth voltage supply lines are intersected and interconnected at the conjunction regions.

29. (Original) The memory device of claim 27

where the charge storing means comprises a decoupling capacitor capable of preventing a power noise caused at a sensing operation.

30. (Original) The memory device of claim 29 where the decoupling capacitor comprises:

an active region formed to surround the core block;

a plurality of first conductive films formed over the active region and connected to the first and third voltage supply lines; and

a second conductive film formed over the active region and connected to the second and fourth voltage supply lines;

where the second conductive film is capable of electrically connecting to the active region through a plurality of contacts.

31. (Currently amended) A semiconductor memory device, comprising:

a core block including a plurality of sub-arrays arranged in rows and columns and a plurality of sense amplifier regions each arranged between sub-arrays adjacent in a column direction;

first and second charge storing regions disposed at a first and second sides, respectively, of the core block, first and second decoupling capacitors being formed at the first and second charge storing regions, respectively;

a plurality of first voltage supply lines connected to first electrodes of the first and second decoupling capacitors, the plurality of first voltage supply lines being capable of supplying a first operating voltage to the sense amplifier regions; and

a plurality of second voltage supply lines connected to second electrodes of the first and second decoupling capacitors, the plurality of second voltage supply lines being capable of supplying a second operating voltage to the sense amplifier regions.

32. (Original) The memory device of claim 31 where the first electrodes of the first and second decoupling capacitors comprises a plurality of conductive films connected to the first voltage supply lines.

33. (Original) The memory device of claim 31 where the second electrodes of the first and second decoupling capacitors comprises a plurality of conductive films connected to the second voltage supply lines.

34. (Original) A semiconductor memory device comprising:

a core block including a plurality of sub-arrays arranged in rows and columns, a plurality of word line driving regions disposed between adjacent sub-arrays, a plurality of sense amplifier regions each arranged between adjacent sub-arrays, and a plurality of conjunction regions each disposed between the sense amplifier regions;

a plurality of first voltage supply lines disposed on sense amplifier and conjunction regions;

a plurality of second voltage supply lines disposed on the sense amplifier and conjunction regions;

a plurality of third voltage supply lines disposed on sense amplifier and word line driving regions;

a plurality of fourth voltage supply lines disposed on the sense amplifier and word line driving regions; and

a charge storing region disposed to surround the core block and having a decoupling capacitor capable of storing a charge;

where the first and third voltage supply lines are connected to the one electrode and the second and fourth voltage supply lines are connected to the another electrode.

35. (Original) The memory device of claim 34

where the first and third voltage supply lines supply a voltage supply voltage to the sense amplifier regions; and

where the second and fourth voltage supply lines supply a ground voltage to the sense amplifier regions.

36. (Original) A semiconductor memory device, comprising:

a core block including a plurality of sub-arrays arranged in rows and columns, a plurality of word line driving regions disposed between adjacent sub-arrays adjacent, a plurality of sense amplifier regions each arranged between adjacent sub-arrays, and a plurality of conjunction regions each disposed between adjacent sense amplifier regions;

a plurality of first voltage supply lines disposed on sense amplifier and conjunction regions;

a plurality of second voltage supply lines disposed on the sense amplifier and conjunction regions;

a plurality of third voltage supply lines disposed on sense amplifier and word line driving regions;

a plurality of fourth voltage supply lines disposed on the sense amplifier and word line driving regions; and

first and second charge storing regions disposed respectively at two sides of the core block and including first and second decoupling capacitors, respectively;

where the third voltage supply lines are connected to first electrodes of the first and second decoupling capacitors and the fourth voltage supply lines are connected to second electrodes of the first and second decoupling capacitor.

37. (Original) The memory device of claim 36

where the first and third voltage supply lines are intersected and interconnected at the conjunction regions; and

where the second and fourth voltage supply lines are intersected and interconnected at the conjunction regions.

38. (Original) The memory device of claim 36 where the first electrodes of the first and second decoupling capacitors comprises a plurality of conductive films connected to the third voltage supply lines.

39. (Original) The memory device of claim 36 where the second electrodes of the first and second decoupling capacitors comprises a plurality of conductive films connected to the fourth voltage supply lines.

40. (New) The memory device of claim 23 where the sense amplifiers are adapted to receive the first and second operating voltages.

41. (New) The memory device of claim 24 where the sense amplifiers are adapted to receive the first and second operating voltages.

42. (New) The memory device of claim 26 where the sense amplifier regions include a plurality of sense amplifiers to receive the first and second operating voltages.